



Panasonic Liquid Crystal Display Co., Ltd.

TENTATIVE

TECHNICAL DATA

VVX32H110G00

CONTENTS

No.	Item	Sheet No.	Page
-	COVER	IPS4PS 2601 -VVX32H110G00-1	1-1/1
-	RECORD OF REVISION	IPS4PS 2602 -VVX32H110G00-1	2-1/1
-	DESCRIPTION	IPS4PS 2603 -VVX32H110G00-1	3-1/1
1	ABSOLUTE MAXIMUM RATINGS	IPS4PS 2604 -VVX32H110G00-1	4-1/2 ~ 2/2
2	INITIAL OPTICAL CHARACTERISTICS	IPS4PS 2605 -VVX32H110G00-1	5-1/2 ~ 2/2
3	ELECTRICAL CHARACTERISTICS	IPS4PS 2606 -VVX32H110G00-1	6-1/1
4	BLOCK DIAGRAM	IPS4PS 2607 -VVX32H110G00-1	7-1/1
5	INTERFACE PIN ASSIGNMENT	IPS4PS 2608 -VVX32H110G00-1	8-1/6 ~ 6/6
6	INTERFACE TIMING	IPS4PS 2609 -VVX32H110G00-1	9-1/3 ~ 3/3
7	DIMENSIONAL OUTLINE	IPS4PS 2610 -VVX32H110G00-1	10-1/5 ~ 5/5

**RECORD OF REVISION**

Date	The upper section : Previous revision The lower section : New revision		Summary
	Sheet No.	Page	



DESCRIPTION

The following specifications are applied to the following TFT module.

Product Name : VVX32H110G00

General Specifications

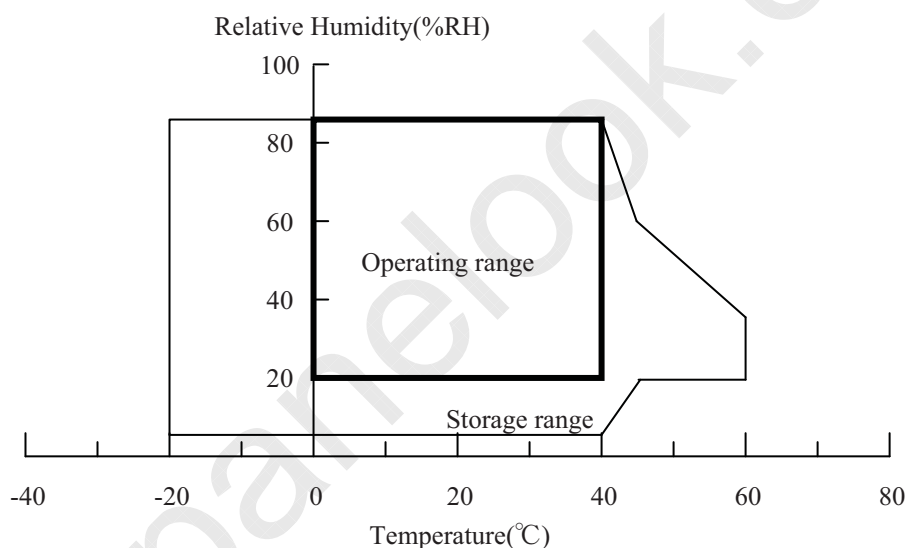
Effective Display Area	: (H)697.685×(V)392.256	(mm)
Number of Pixels	: (H)1,366×(V)768	(pixels)
Pixel Pitch	: (H)0.51075×(V)0.51075	(mm)
Color Pixel Arrangement	: R+G+B Vertical Stripe	
Display Mode	: Transmissive Mode Normally Black Mode	
Top Polarizer Type	: Semi-Glare	
Number of Colors	: 16,777,216	(colors)
Viewing Angle Range	: Wide Version (Horizontal & Vertical : 178°at φ=0°,90°, 180°,270°, CR≥10)	
Input Signal	: 1-channel LVDS (LVDS:Low Voltage Differential Signaling)	
Back Light	: Edge LED Type	
External Dimensions	: Typ. (H) 735.4 × (V) 433.0 × (t) 25.1	(mm)
Weight	: TBD	(g)

1. ABSOLUTE MAXIMUM RATINGS

1.1 Environmental absolute maximum ratings

ITEM	Operating		Storage		UNIT	NOTE
	Min.	Max.	Min.	Max.		
Temperature	0	50	-20	60	°C	1),5),6)
Humidity	2)		2)		%RH	1)
Vibration	-	4.9(0.5 G)	-	9.8(1.0G)	m/s ²	3)
Shock	-	29.4(3 G)	-	196(20G)	m/s ²	4)
Corrosive gas	Not acceptable		Not acceptable		-	

- Note 1) Temperature and Humidity should be applied to the glass surface of a IPS-Pro TFT LCD module, not to the system installed with a module.
The brightness of a CCFL tends to drop at low temperature. Besides, the life-time becomes shorter at low temperature.
- 2) $T_a \leq 40^\circ\text{C}$ ······Relative humidity should be less than 85 %RH max. Dew is prohibited.
 $T_a > 40^\circ\text{C}$ ······Relative humidity should be lower than the moisture of the 85 %RH at 40°C .



- 3) Frequency of the vibration is between 15 Hz and 100 Hz. (Remove the resonance point)
- 4) Pulse width of the shock is 10 ms.
- 5) Long operation under low temperature may cause some portion of display area to be reddish for several minutes after turning on the product.
However, it does not affect the characteristics and reliability of the product.
- 6) The temperature of LCD front surface would be 65°C in operating, it may affect the optical characteristics however it does not damage the function of the module.

1. 2 Electrical absolute maximum ratings

(1)TFT-LCD module

V_{SS} = 0 V

ITEM	SYMBOL	Min.	Max.	UNIT	NOTE
Power supply voltage	V _{DD}	0	13.2	V	
Input voltage for logic	V _I	-0.3	3.6	V	1)
Electrostatic durability	V _{ESD0}	±100		V	2),3)
	V _{ESD1}	±8		kV	2),4)

Note 1) It is applied to pixel data signal and clock signal.

2) Discharge coefficient : 200 pF - 250 Ω, Environmental : 25 °C - 70%RH

3) It is applied to I/F connector pins.

4) It is applied to the surface of a metallic bezel and a LCD panel.

(2) Back-light Driver

V_{SS} = 0 V

ITEM	SYMBOL	Min.	Max.	UNIT	NOTE
Input voltage	V _{in}	0	26.4	V	
ON/OFF control input voltage	ON/OFF	0	5.0	V	
PWM signal voltage	V _{pwm}	0	5.0	V	

2. INITIAL OPTICAL CHARACTERISTICS

The following optical characteristics are measured under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted.

The optical characteristics should be measured in a dark room or equivalent state.

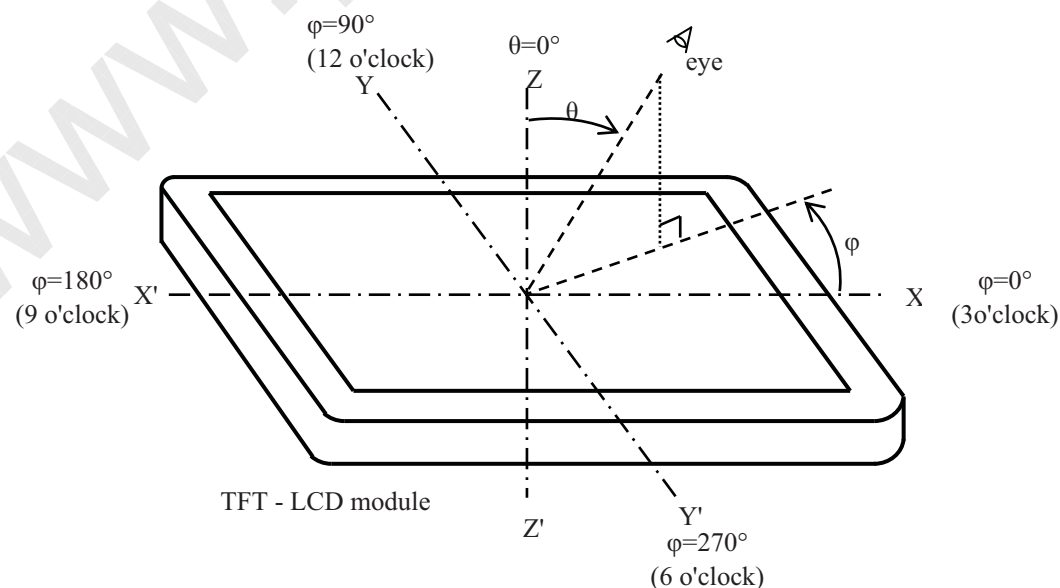
Measuring equipment : CS-1000A, or equivalent

Ambient Temperature =25 °C , VDD=12.0 V , f v=60 Hz ,

V_{in}=24V , PWM on duty =100 %

ITEM		SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT	NOTE
Contrast ratio		CR	$\theta = 0^\circ$ 1)	700	1200	-	-	2)
Response time	Rise	ton		-	8	20	ms	3)
	Fall	toff		-	6	20	ms	3)
Brightness of white		Bwh		250	350	-	cd/m ²	
Brightness uniformity		Buni		-	-	30	%	4)
Color chromaticity (CIE)	Red	x		0.615	0.645	0.675	-	【Gray scale =255】
		y		0.300	0.330	0.360		
	Green	x		0.270	0.300	0.330		
		y		0.590	0.620	0.650		
	Blue	x		0.123	0.153	0.183		
		y	0.035	0.065	0.095			
	White	x	0.248	0.278	0.308			
		y	0.255	0.285	0.315			
Variation of color position (CIE)	Red	Δx	$\theta = +50^\circ$ $\varphi = 0^\circ, 90^\circ, 180^\circ, 270^\circ$ 1)	-	-	0.04	-	5) 【Gray scale =255】
		Δy		-	-	0.04		
	Green	Δx		-	-	0.04		
		Δy		-	-	0.04		
	Blue	Δx		-	-	0.04		
		Δy		-	-	0.04		
	White	Δx		-	-	0.04		
		Δy		-	-	0.04		
Contrast ratio at 89 °		CR89	6)	10	-	-	-	Estimated value

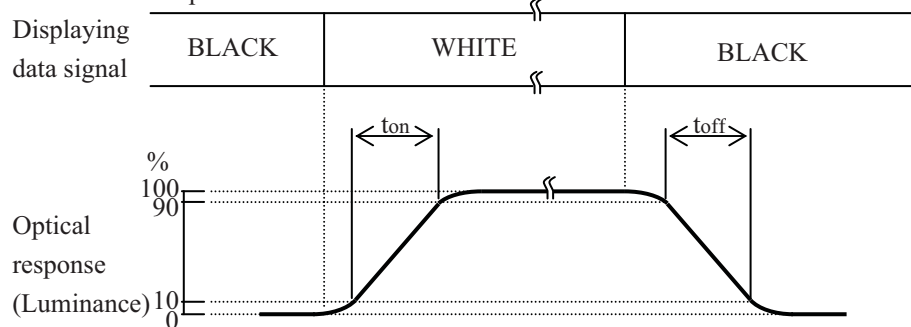
Note 1) Definition of viewing angle



Note 2) Definition of contrast ratio (CR)

$$CR = \frac{(\text{Luminance at displaying WHITE})}{(\text{Luminance at displaying BLACK})}$$

3) Definition of response time



4) Definition of brightness uniformity

Display pattern is white (255 level). The brightness uniformity is defined as the following equation.

Brightness at each point is measured, and average, maximum and minimum brightness is calculated.

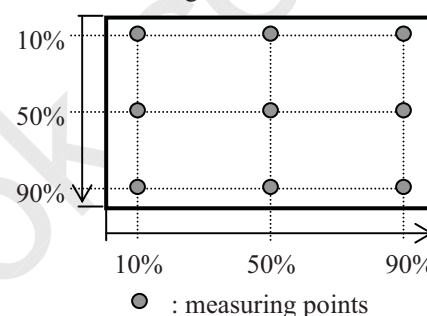
$$B_{uni} = \frac{|B_{max} \text{ or } B_{min} - B_{ave}|}{B_{ave}} \times 100$$

where, B_{max} = Maximum brightness

B_{min} = Minimum brightness

B_{ave} = Average brightness

$$B_{ave} = \frac{\sum_{k=1}^9 (B(k))}{9}$$



5) Variation of color position on CIE

Variation of color position on CIE is defined as difference between colors at $\theta = 0^\circ$ and at $\theta = 50^\circ$ & $\phi = 0^\circ, 90^\circ, 180^\circ, 270^\circ$.

6) Contrast ratio at 89°

Evaluation conditions are on horizontal & vertical axis

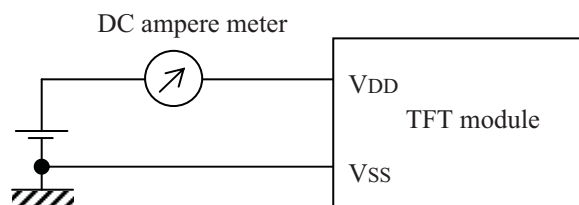
3. ELECTRICAL CHARACTERISTICS

3.1 TFT-LCD module

$T_a = 25\text{ }^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$

ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Power supply voltage	V_{DD}	11.4	12.0	12.6	V	
Power supply current	I_{DD}	-	0.4	0.8	A	1),2)
Ripple voltage of power supply	V_{DDR}	-	-	350	mV	

Note 1) $f_v=60.0\text{Hz}$, $f_{CLK}=85\text{MHz}$, $V_{DD}=12.0\text{V}$, and display pattern is horizontal stripe.



- 2) Current fuse is built in a module. Current capacity of power supply for V_{DD} should be larger than 4A, so that the fuse can be opened at the trouble of electrical circuit of module.

3.2 Back light unit

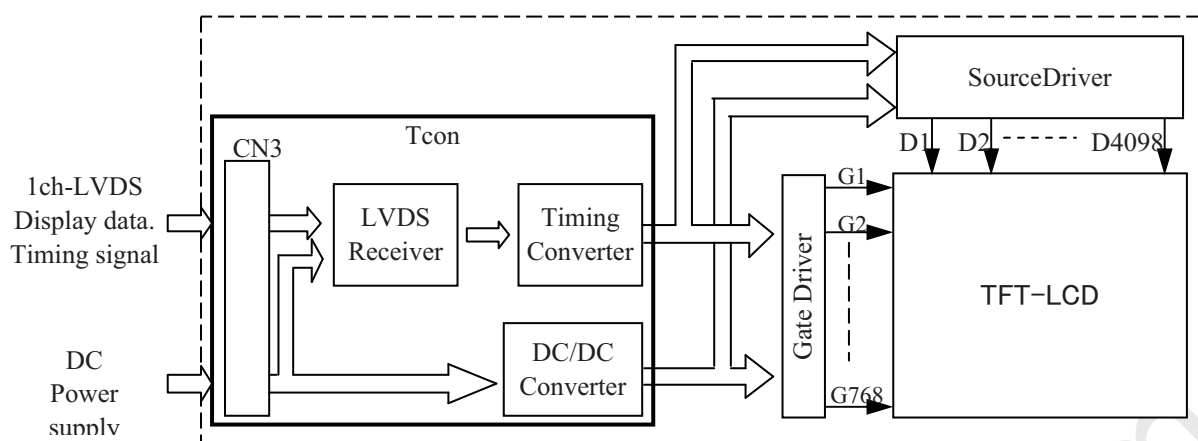
$T_a = 25\text{ }^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$

ITEM		SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Input voltage		V_{in}	21.6	24.0	26.4	V	
Input current		I_{in}	-	(1.4)	-	A	PWM on-duty=100% $V_{in}=24\text{V}, 120\text{Hz}$
ON/OFF Control voltage	ON	ON/OFF	2.0	3.3	5.0	V	
	OFF		0	-	0.8		
PWM signal	Low	V_{pwm}	0	-	0.8	V	
	High		2.0	-	3.3		
PWM frequency		-	90	120	360	Hz	
On-duty range for burst-dimming		On-duty	0	-	100	%	

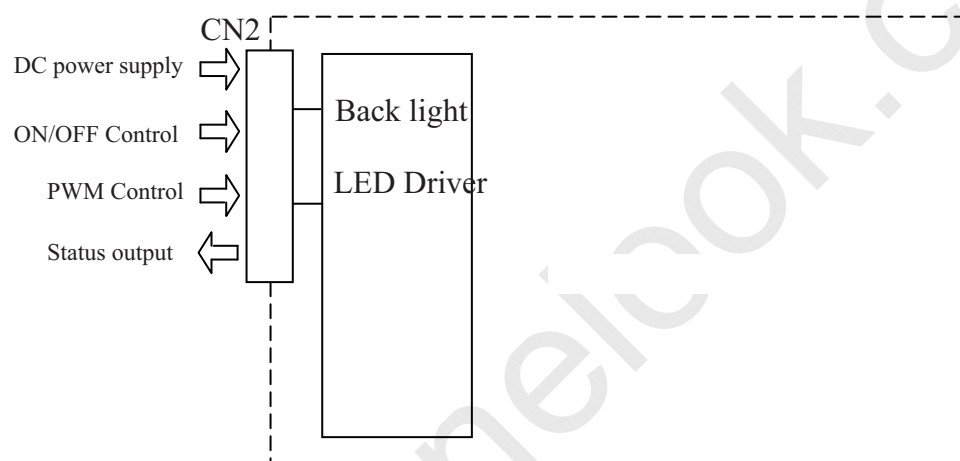
Note 1) This characteristics should be applied putting on the LED about 60 minutes later with ambient temperature.
($T_a = 25\text{ }^{\circ}\text{C} \pm 2\text{ }^{\circ}\text{C}$)

4. BLOCK DIAGRAM

4.1 TFT-LCD module



4.2 Back light unit



**5. INTERFACE PIN ASSIGNMENT****5.1 TFT-LCD MODULE**

CN3:JAE FI-X30SSLA-HF or FI-X30SSL-HF

(Matching connector : JAE FI-X30C2L)

Pin No.	SYMBOL	Description	Note
1	VDD	Power Supply (typ.+12V)	1)
2	VDD		
3	VDD		
4	VDD		
5	VSS	GND(0V)	2)
6	VSS		
7	VSS		
8	VSS		
9	IC	Internally Connected, Keep Open	
10	IC		
11	VSS	GND(0V)	
12	Rx0-	Pixel Data	3)
13	Rx0+		
14	VSS	GND(0V)	2)
15	Rx1-	Pixel Data	3)
16	Rx1+		
17	VSS	GND(0V)	2)
18	Rx2-	Pixel Data	3)
19	Rx2+		
20	VSS	GND(0V)	2)
21	CLK-	Pixel Data	3)
22	CLK+		
23	VSS	GND(0V)	2)
24	Rx3-	Pixel Data	3)
25	Rx3+		
26	VSS	GND(0V)	2)
27	NC	No Connection	
28	NC	No Connection	
29	NC	No Connection	
30	VSS	GND(0V)	2)

Notes 1) All VDD pins shall be connected to +12.0V(Typ.).

2) All VSS pins shall be grounded. Metal bezel is internally connected to VSS.

3) Rx n+ and Rx n- (n=0,1,2,3) should be wired by twist-pairs or side-by-side FPC patterns, respectively.



5.2 Back light unit

Inverter pin assignment

JST S14B-PHA-SM-TB(LF)(SN)

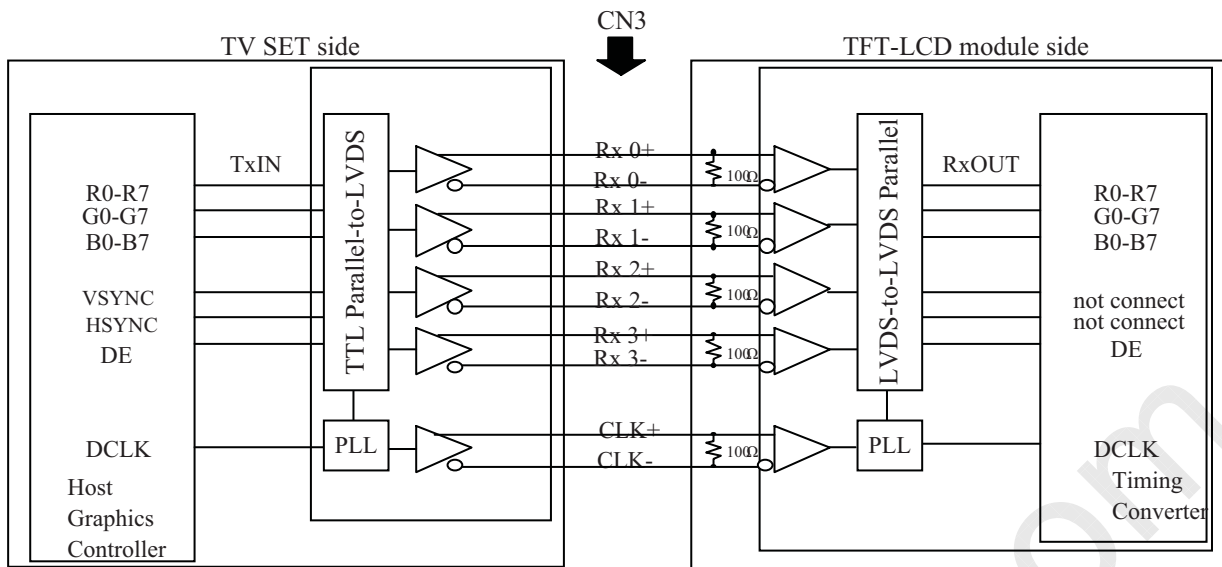
(Matching connector : JST PHR-14)

PIN No.	SYMBOL	DESCRIPTION	NOTE
1	Vin	Power supply (Typ. +24.0V)	1)
2	Vin		
3	Vin		
4	Vin		
5	Vin		
6	Vss	GND (0V)	2)
7	Vss		
8	Vss		
9	Vss		
10	Vss		
11	FAIL	Status output (Normal:GND abnormal:open)	
12	ON/OFF	High : LED ON(3.3V) Low : LED OFF	
13	IC	Internally Connected, Keep Open	
14	PWM	0-3.3V pulse	

Note 1) All Vin pins shall be connected to +24.0V(Typ.).

2) All Vss pins shall be grounded. Metal bezel is internally connected to Vss.

5.3 Block diagram of interface



R0~R7 : Pixel R Data (7; MSB, 0; LSB)
 G0~G7 : Pixel G Data (7; MSB, 0; LSB)
 B0~B7 : Pixel B Data (7; MSB, 0; LSB)
 DE : Data Enable

- Note 1) The system must have the transmitter to drive the module.
 2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5. 4 LVDS interface

	SIGNAL	TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER		TFT CONTROL
		PIN	INPUT	TV Set	TFT-LCD	PIN	OUTPUT	INPUT
24bit	R0	51	Tx IN0	TA OUT0+	Rx 0+	27	Rx OUT0	R0
	R1	52	Tx IN1			29	Rx OUT1	R1
	R2	54	Tx IN2			30	Rx OUT2	R2
	R3	55	Tx IN3			32	Rx OUT3	R3
	R4	56	Tx IN4	TA OUT0-	Rx 0-	33	Rx OUT4	R4
	R5	3	Tx IN6			35	Rx OUT6	R5
	G0	4	Tx IN7			37	Rx OUT7	G0
	G1	6	Tx IN8			38	Rx OUT8	G1
	G2	7	Tx IN9	TA OUT1+	Rx 1+	39	Rx OUT9	G2
	G3	11	Tx IN12			43	Rx OUT12	G3
	G4	12	Tx IN13			45	Rx OUT13	G4
	G5	14	Tx IN14			46	Rx OUT14	G5
	B0	15	Tx IN15	TA OUT1-	Rx 1-	47	Rx OUT15	B0
	B1	19	Tx IN18			51	Rx OUT18	B1
	B2	20	Tx IN19			53	Rx OUT19	B2
	B3	22	Tx IN20			54	Rx OUT20	B3
	B4	23	Tx IN21	TA OUT2+	Rx 2+	55	Rx OUT21	B4
	B5	24	Tx IN22			1	Rx OUT22	B5
	HSYNC	27	Tx IN24			3	Rx OUT24	not connect
	VSYNC	28	Tx IN25	TA OUT2-	Rx 2-	5	Rx OUT25	not connect
	DE	30	Tx IN26			6	Rx OUT26	DE
	R6	50	Tx IN27			7	Rx OUT27	R6
	R7	2	Tx IN5	TA OUT3+	Rx 3+	34	Rx OUT5	R7
	G6	8	Tx IN10			41	Rx OUT10	G6
	G7	10	Tx IN11			42	Rx OUT11	G7
	B6	16	Tx IN16			49	Rx OUT16	B6
	B7	18	Tx IN17	TA OUT3-	Rx 3-	50	Rx OUT17	B7
	RSVD 1)	25	Tx IN23			2	Rx OUT23	not connect
	DCLK	31	TxCLK IN	TxCLK OUT+	RxCLK IN+	26	RxCLK OUT	DCLK
				TxCLK OUT-	RxCLK IN-			

R0~R7 : Pixel R Data (7; MSB, 0; LSB)

G0~G7 : Pixel G Data (7; MSB, 0; LSB)

B0~B7 : Pixel B Data (7; MSB, 0; LSB)

DE : Data Enable

Note 1) RSVD (reserved) pins on the transmitter shall be tied to"H"or"L".

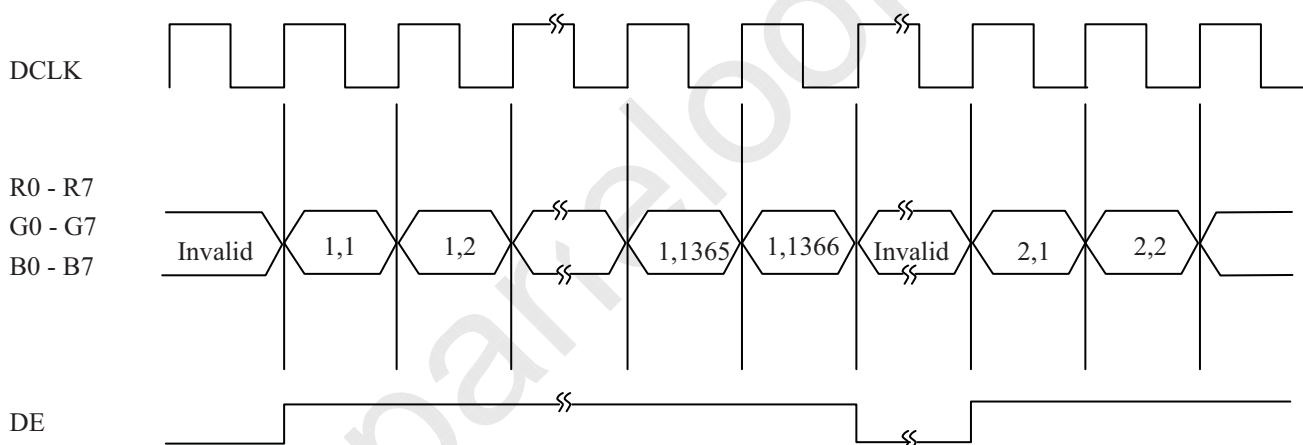
5. 5 Correspondence between input data and display image

Display data of adjacent one pixel is latched during one cycle of DCLK.

	(1,1)	
R	G	B

Pixel : R0 - R7 : R data
G0 - G7 : G data
B0 - B7 : B data

768 , 1366	768 , 1365	768 , 1364	-----	768 , 1
767 , 1366	767 , 1365	767 , 1364	-----	767 , 1
766 , 1366	766 , 1365	766 , 1364	-----	766 , 1
⋮	⋮	⋮		⋮
1 , 1366	1 , 1365	1 , 1364		1 , 1





5. 6 Relationship between display colors and input signals

Input Color		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB								LSB								MSB							
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note 1) Definition of gray scale :

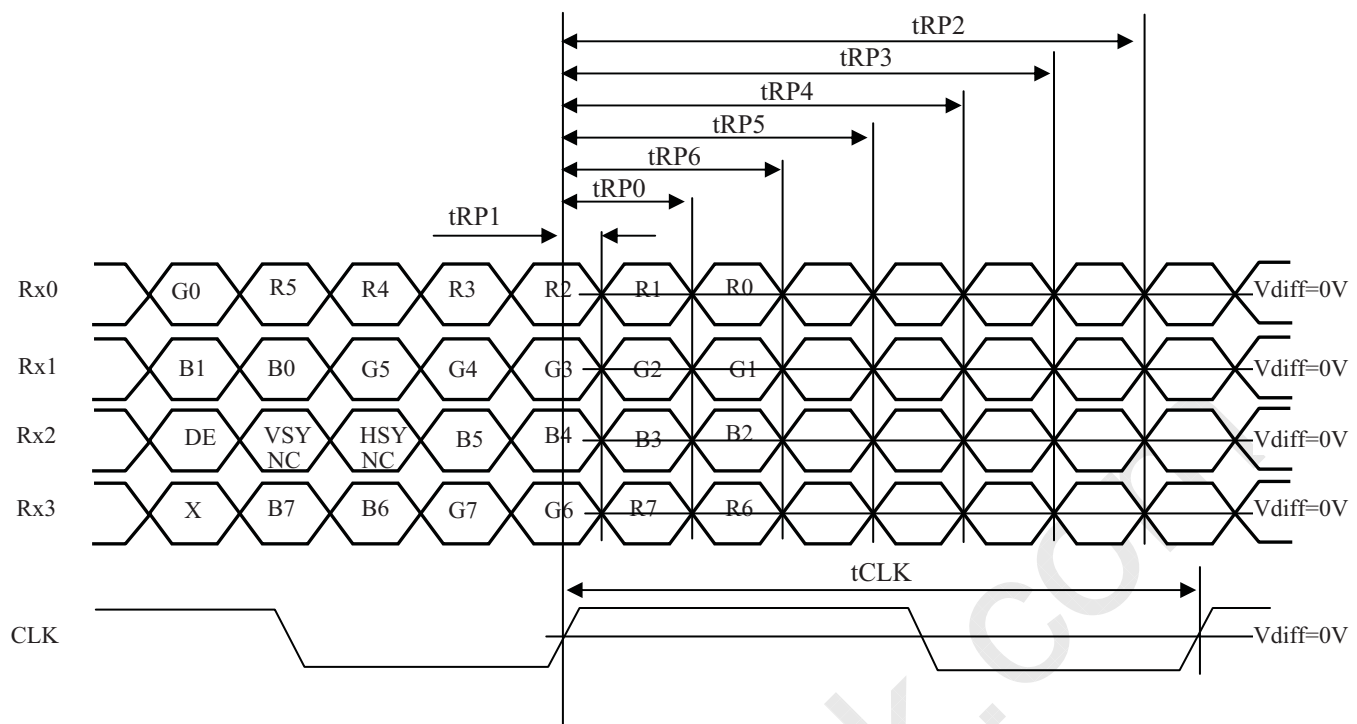
Color(n) · · · · Number in parenthesis indicates gray scale level.

Larger n correspondsto brighter level.

2) Data : 1 : High, 0 : Low

6. INTERFACE TIMING

6.1 LVDS receiver timing



$$Rx0=(Rx0+)-(Rx0-)$$

$$Rx1=(Rx1+)-(Rx1-)$$

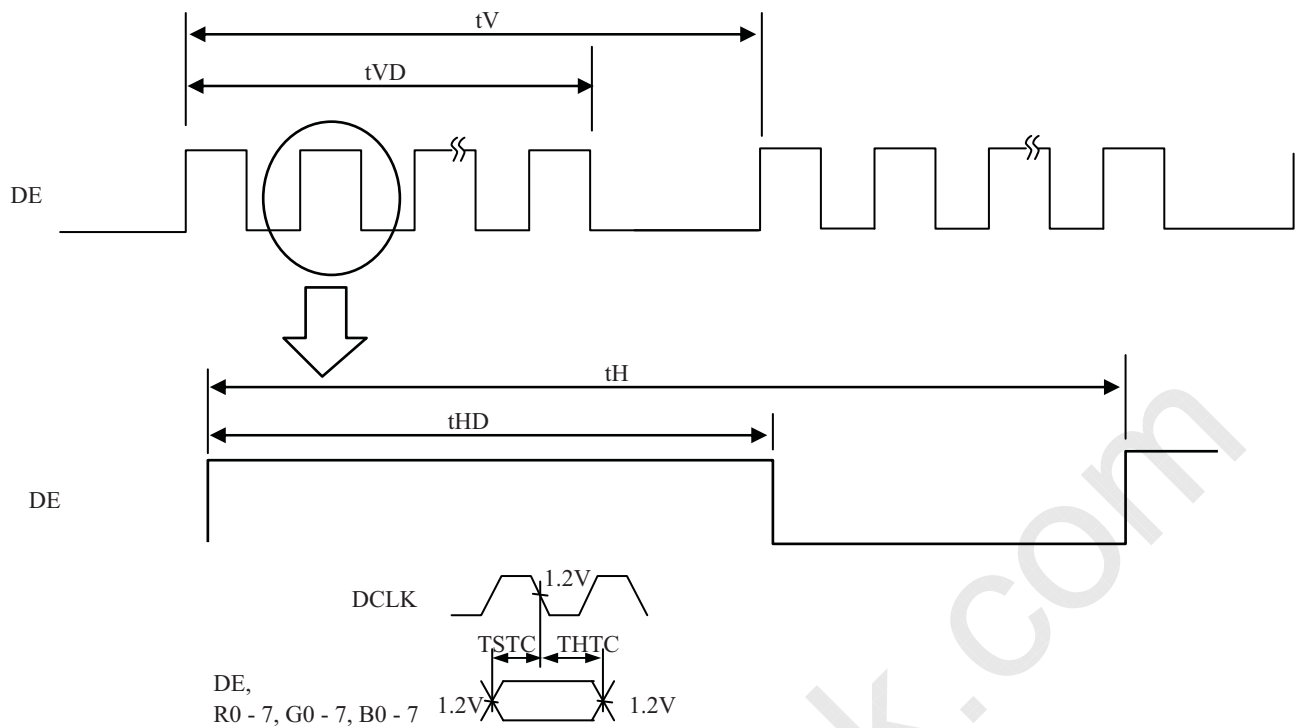
$$Rx2=(Rx2+)-(Rx2-)$$

$$Rx3=(Rx3+)-(Rx3-)$$

$$CLK=(CLK+)-(CLK-)$$

ITEM		SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
CLK	Frequency (at 50 Hz)	DCLK	68	78	87	MHz	
	Frequency (at 60 Hz)		78	85	87	MHz	
Rx*0 Rx*1 Rx*2 Rx*3	0 data position	tRP0	$1/7tCLK - 0.4$	$1/7tCLK$	$1/7tCLK + 0.4$	ns	
	1st data position	tRP1	- 0.4	0	+ 0.4		
	2nd data position	tRP2	$6/7tCLK - 0.4$	$6/7tCLK$	$6/7tCLK + 0.4$		
	3rd data position	tRP3	$5/7tCLK - 0.4$	$5/7tCLK$	$5/7tCLK + 0.4$		
	4th data position	tRP4	$4/7tCLK - 0.4$	$4/7tCLK$	$4/7tCLK + 0.4$		
	5th data position	tRP5	$3/7tCLK - 0.4$	$3/7tCLK$	$3/7tCLK + 0.4$		
	6th data position	tRP6	$2/7tCLK - 0.4$	$2/7tCLK$	$2/7tCLK + 0.4$		

6.2 Synchronization signal timing



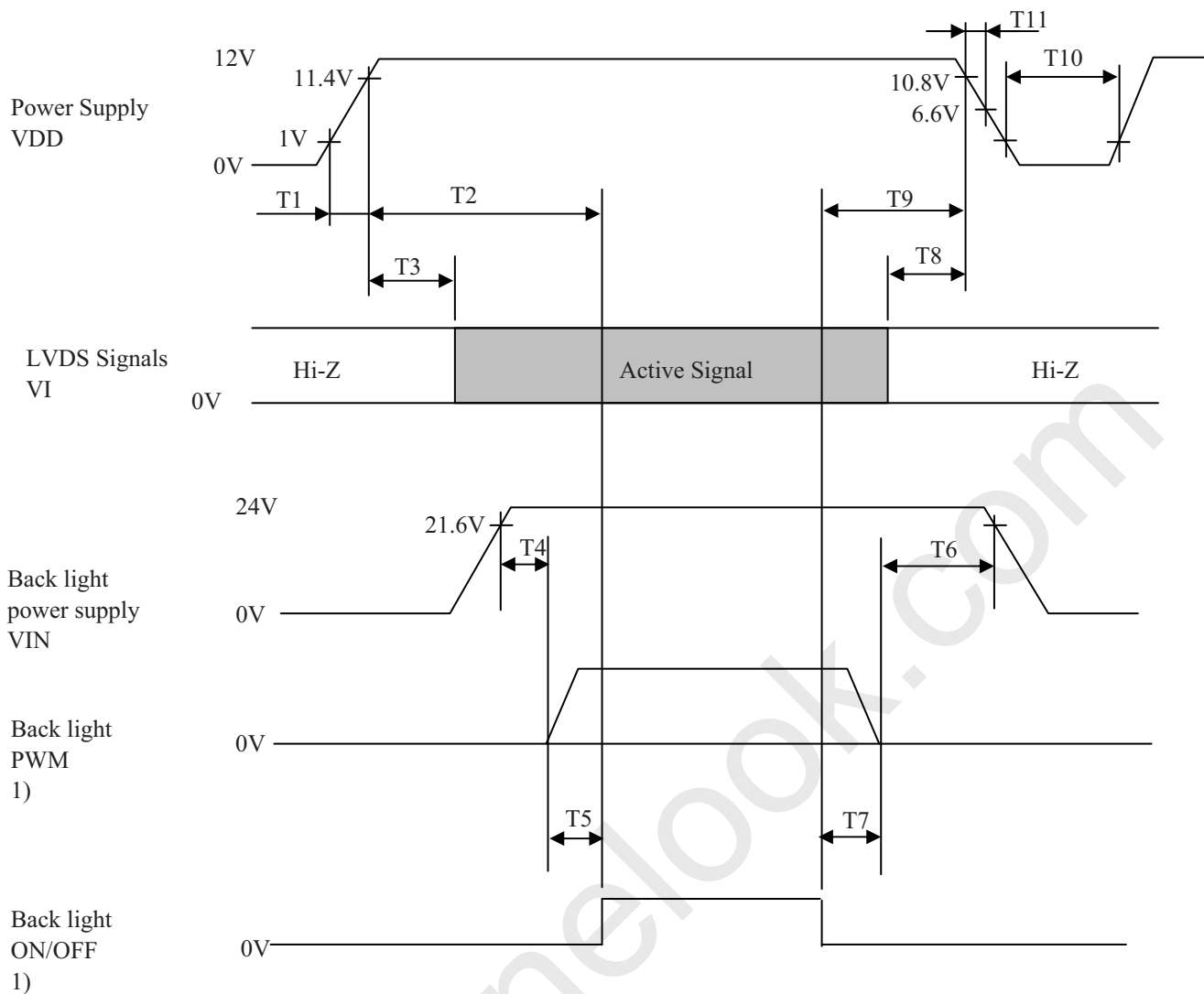
Note 1) Reference level for each timing signal is 1.2 V unless it is stated on the chart, high level voltage(VIH) and low level voltage(VIL) are defined as follows:

$$V_{IH} \geq 2.0 \text{ V} \quad V_{IL} \leq 0.8 \text{ V}$$

2) The timing of DCLK to other signals conforms to the specifications of LVDS transmitter.

ITEM		SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
DE	Vertical frequency	fV	46	50 / 60	62	Hz	
	Vertical period	tV	773	860 / 800	1050	tH	
	Vertical valid	tVD	768			tH	
	V-Blanking	-	5	92 / 32	282	tH	
	Horizontal frequency	fH	39.6	43 / 48	49.6	kHz	
	Horizontal period	tH	1400	1814 / 1771	2000	tCLK	
	Horizontal valid	tHD	1366			tCLK	
	H-Blanking	-	34	448 / 405	634	tCLK	

6.3 Timing between interface signals power supply



$$0 \leq T1 \leq 10$$

$$350 \leq T2$$

$$10 \leq T3$$

$$200 \leq T4$$

$$200 \leq T5$$

$$0 \leq T6$$

$$0 \leq T7$$

$$0 \leq T8$$

$$0 \leq T9$$

$$350 \leq T10$$

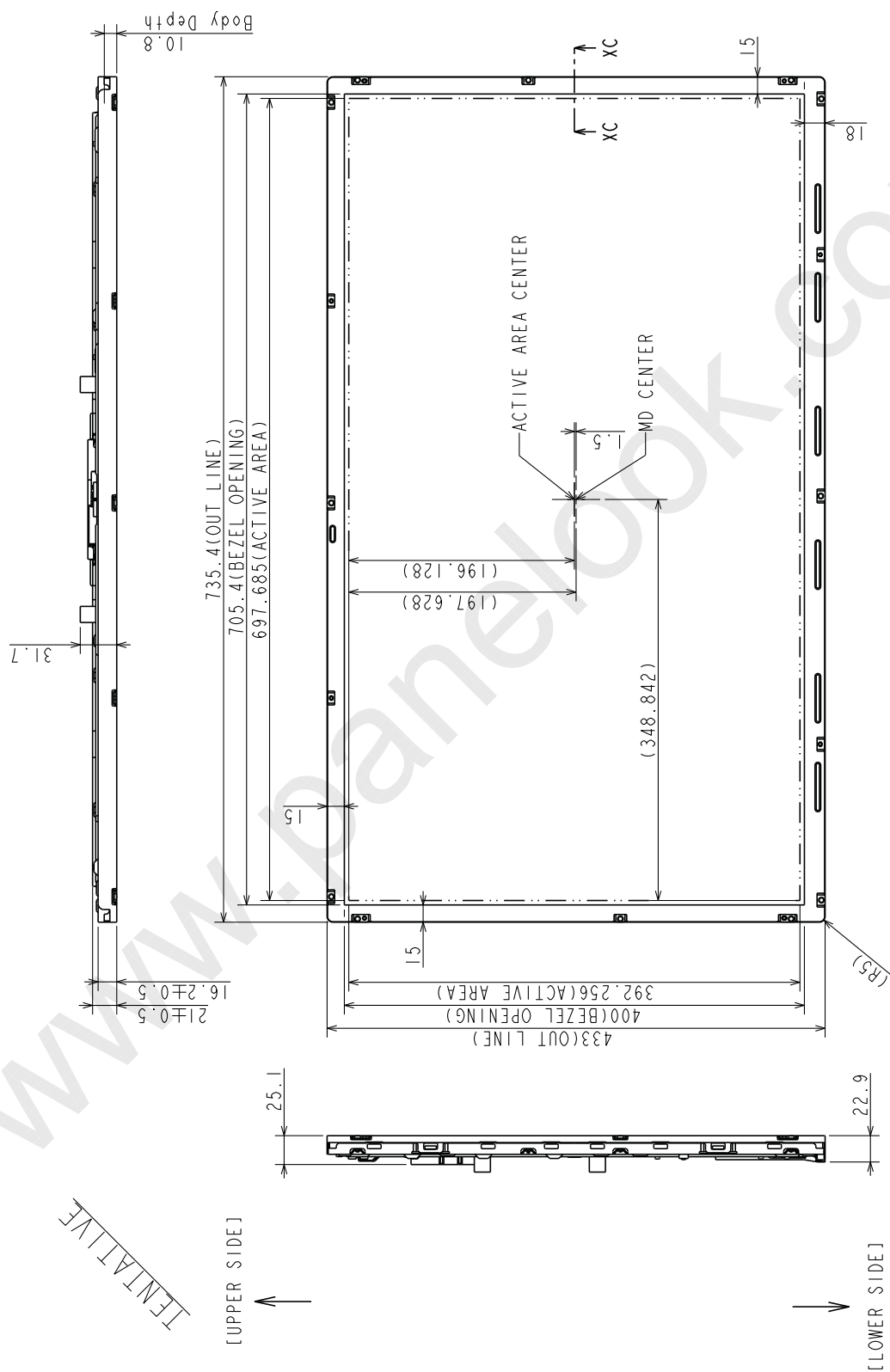
$$10 < T11$$

Unit : ms

Note 1) In all periods, the backlight ON/OFF signal voltage and the PWM signal voltage should be lower than the backlight power supply voltage.

7. DIMENSIONAL OUT LINE

(1) FRONT VIEW



Note 1) The dimension in a parenthesis is a reference value.

2) Unspecified tolerance to be ± 0.8

3) The measuring method depends on IPS Alpha Technology. standard.

Panasonic
Liquid Crystal Display Co., Ltd.

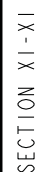
Date _____

Oct. 08, 2010

Sh.	No.
-----	-----

IPS4PS 2610-VVX32H110G00-1

Page 10-1/5

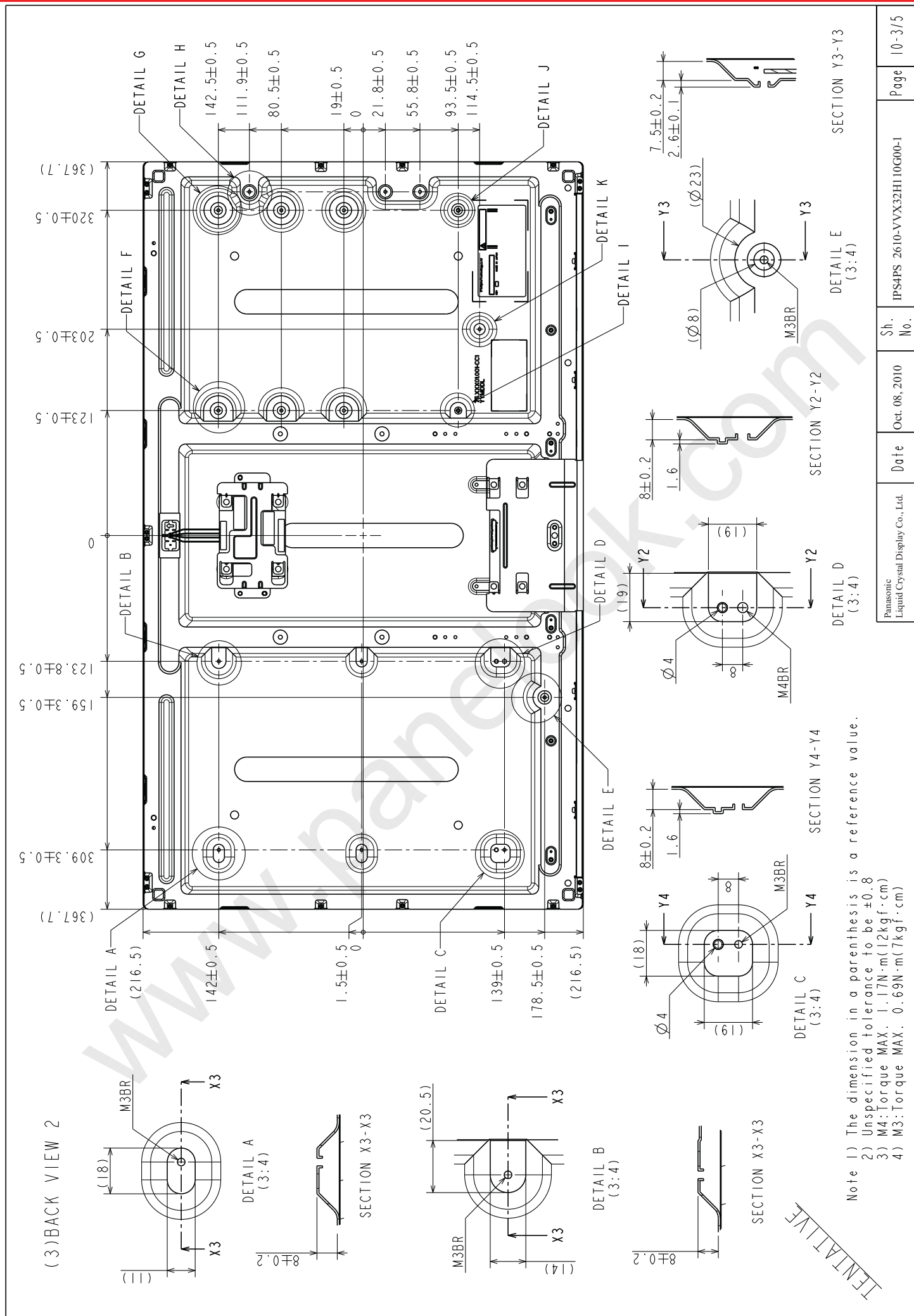


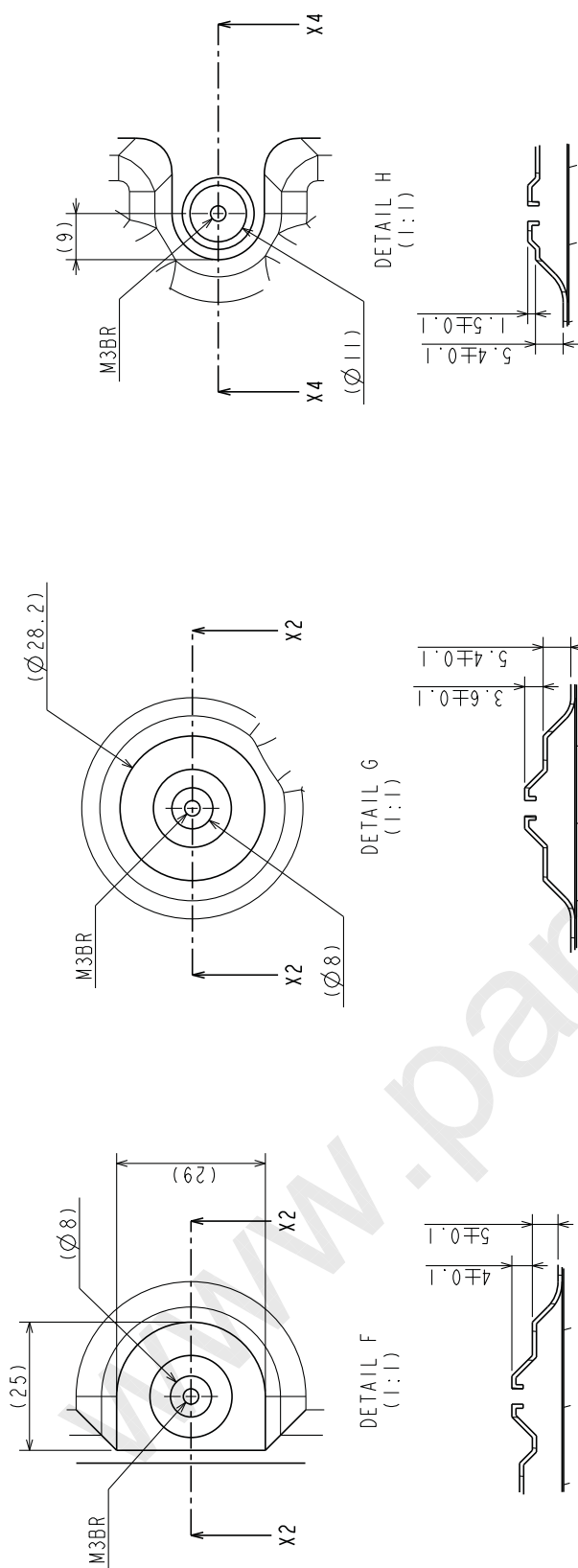
2) Unspecified tolerance to be ± 0.8

3) M4: Torque MAX. 1.17N·m(12kgf·cm)

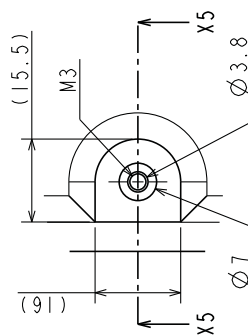
4) M3: Torque MAX. 0.69N·m(7kgf·cm)

Panasonic Liquid Crystal Display Co., Ltd.	Date	Oct. 08, 2010	Sh. No.	IPS4PS 2610-VVX32H110G00-1	Page	10-2/5
---	------	---------------	------------	----------------------------	------	--------

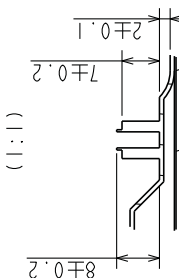




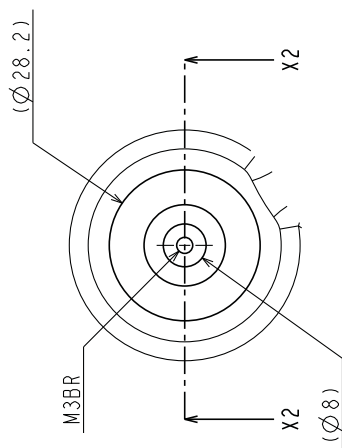
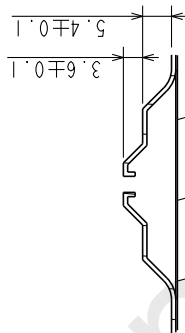
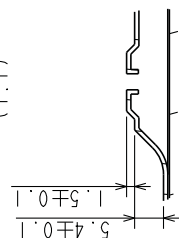
SECTION X2-X2

DETAIL I
(1:1)

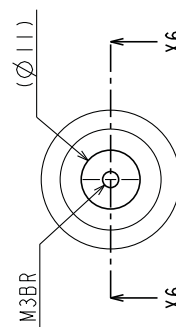
SECTION X5-X5

DETAIL J
(1:1)

SECTION X5-X5

DETAIL G
(1:1)DETAIL H
(1:1)DETAIL K
(1:1)

SECTION X6-X6



SECTION X4-X4

Note 1) The dimension in a parenthesis is a reference value.

2) Unspecified tolerance to be ± 0.8

3) M4: Torque MAX. 1.17N·m (12kgf·cm)

4) M3: Torque MAX. 0.69N·m (7kgf·cm)

Panasonic
Liquid Crystal Display Co., Ltd.

Date

Oct. 08, 2010

Sh.
No.

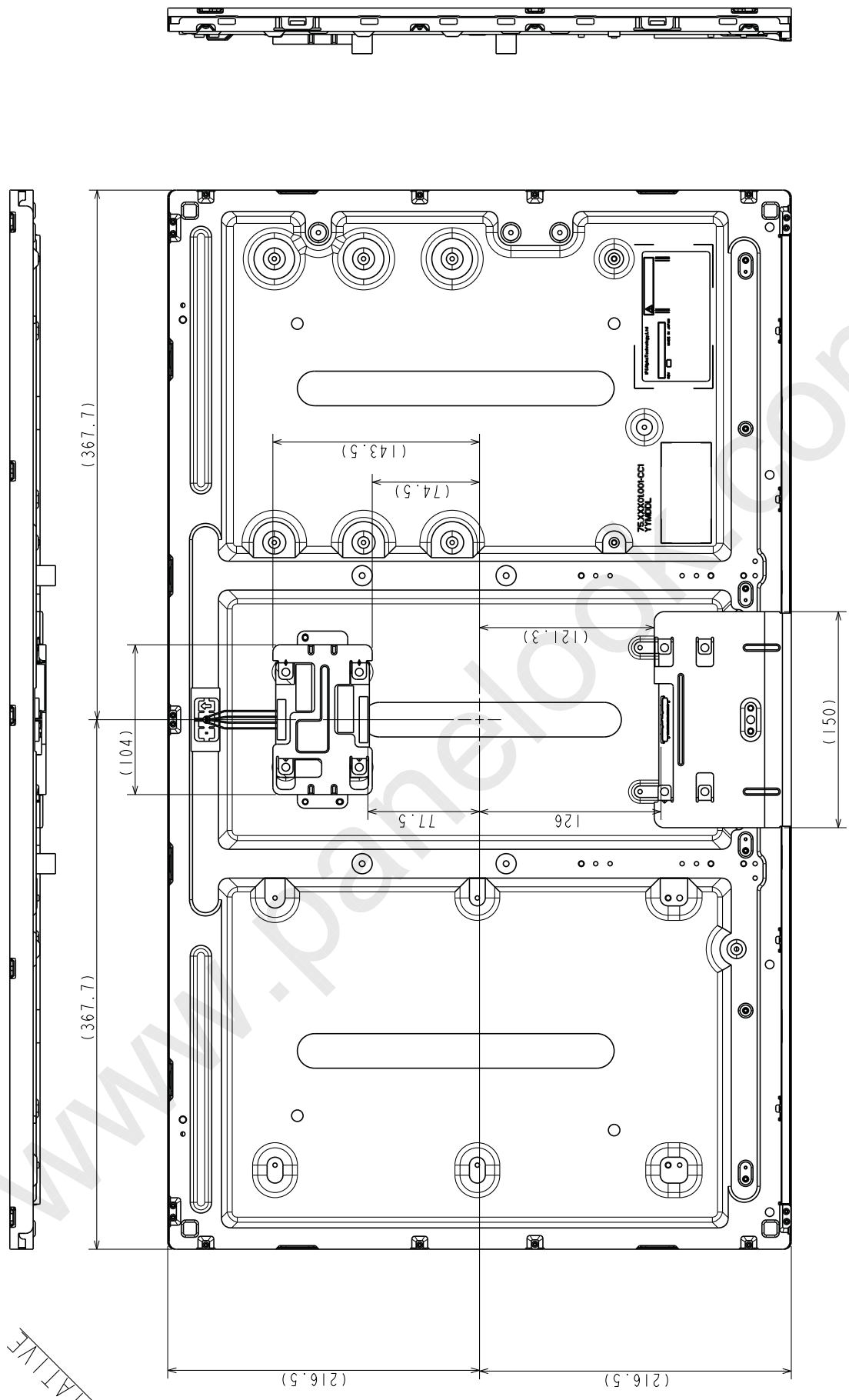
IPS4PS 2610-VVX32H110G00-1

Page

10-4/5

(4)BACK VIEW 3

TENTATIVE



Note 1) The dimension in a parenthesis is a reference value.
2) Unspecified tolerance to be ± 0.8

Panasonic Liquid Crystal Display Co., Ltd.	Date	Oct. 08, 2010	Sh. No.	IPS4PS 2610-VVX32H110G00-1	Page	10-5/5
---	------	---------------	------------	----------------------------	------	--------